off. At this time decoder output line S has to be on. The output line Q_{mn} of the mn-th flip-flop becomes the control input of the mn-th analog switching gate G_{mn}. The detail circuit of this known digital controled analog gate is shown on gate G_{2n} where 4 diodes, 3 transistors and Zener diode (ZD) are used. The input signal must not exceed the range $-E$ to $+E$. The transist $-E$ is always on. When the digital input from FF is high (1), the transistor connected to $+E$ is on. The input and output points in the diamond shaped diodes acts essentially like short circuit (since low forward drops of the diodes). When digital input from FF is low (0), the top transistor is on, and $+E$ transistor is off, Four diodes are reverse biased and produces very high impedence output.

The top blocks are distributors which distribute analog input I to $I_1, \ldots I_n$ after input amplifier. This input amplifier provides signal conditioning in the form of gain trim, dc restoration, and input loss equalization. The input I_{mn} will flow to output O_{mn} through gate G_{mn} when FF_{mn} is on. The output lines $O_{1j}, O_{2j}, \ldots, O_{mj}$ merge to become output O_j. Hence, normally not more than one of the $O_{1j}, \ldots, O_{mj}$ should be on.

A communication control logic (CCL) and communication control table (CCT) must be maintained in the ACC to avoid invalid input array $A_1, \ldots, A_k$ to prevent more than one gate of $G_{1i}, G_{2i}, \ldots, G_{mi}$ to be on for each integer i between 1 and n, unless the mixing of the signals is desired. In other words, CCT contains the current on/off status of each gate G_{ij}, input I_i and output O_j. CCL contains the logic to execute the rules previously mentioned and others such as certain input or output terminals are permanent off, one input may or may not connect to several or certain output terminals, and set priority among the terminals or paths. For example, when CPU requests a path from I_i to O_j, CCL will look the CCT to see if G_{ij} is on and $G_{1j}, G_{2j}, \ldots G_{mj}$ are off. If those rules and others being satisfied then an address set $A_1, \ldots, A_k$ is generated G_{ij} set on and CCT is updated. Otherwise, CPU is notified that the request is rejected.

In addition, with the programability, it is easy to add to the ACC more functions such as tally (to indicate which terminals are on currently) and monitory (communication statistics).

When ACC has to handle bidirectional communication, two ACCs can be used. One ACC controlling one direction and the other one controlling the other direction.

If the number of inputs m and the number of outputs n are large, the number of gates and the number of paths mxn used in the ACC described before can be too large to be practical. Besides, in many applications the maximum number of input terminals being on at any time is considerably smaller than m. In this case additional serial ACCs can reduce the number of gates and total length of paths dramatically. For example if $m=60$, $n=70$ and if the maximum number of input terminals being on at any time is 10, two ACCs needed are 60 to 10 and 10 to 70. The total number of paths or gates of those two ACCs is 1300 which is much less than one ACC of 4200 paths or gates. If the communication distance between those 60 input terminals and those 70 output terminals is large, additional saving on cable lines is huge: 130 units vs. 10 units. Therefore, ACC is a building block for many analog communication control systems. This concept of ACC can be applied to digital communication. The only components changed are that the gates will be pure digital gates. The multiplexing is another powerful way to increase the efficiency in digital communication.

SYSTEM BLOCK DIAGRAM (FIG. 22)

The system block diagram is shown on FIG. 22 to show the control mechanism of major components. Like digital computer, the digital/analog computer also is controlled by the CPU. (For the parallel processor, a plural number of CPUs may be used) There is one digital/analog Memory Pack Accessor per digital/analog memory pack. The digital/analog Memory Pack Accessor is between CPU and other devices such as RAM, TMP (transporter micro processor), VSC (video servo controller), mount/unmount motor which is belong to that particular pack. The current position or status of the shuttle, tape drivers, are stored and constantly updated in the current position table (CPT) which is part of the Digital/analog Memory Pack Accessor controller's memory. But the current tape position for each tape in the pack is stored in CTPT (current tape position table). CTPT is stored in RAM of the memory pack. The analog (video) buffer controller is directly controled by CPU (through scheduler) not through the pack accessor controller. The analog (video) buffer is not directly controled by buffer controller, it is through ACC and buffer servo controller.

SYSTEM FLOW DIAGRAM (FIG. 23)

FIG. 23 is the system flow diagram to show the scheduler and its relation to other components. The digital data is entered via digital monitor. If no corresponding record can be found in RAMs, CPU will send the rejection message back. Otherwise, corresponding internal record ID will then be found in a RAM by CPU. The Tape Operation System then use this ID, which contains pack ID cassette ID and record address in the tape, to locate the corresponding analog record. At mean time CPU will access the digital application data of said found record from RAM and display back to digital terminal. With the information from Tape Access Method, TOS trys to decompose the analog processing job into task cycles and schedule those tasks, one after another. On the scheduled execution time, the right transporter will pick up one of the N x M cassettes to an available player, fast forward the tape to the right position and fast copy segments of record to the available buffers. The buffers will read the copied segments, transmit to the destination terminal under the control of Analog Communication Controller. The ACC is controled by CPU under the TOS and its resources scheduler.

The address data from head drum will help the motor to position the tape at accurate field before process the tape.

GLOBAL AND LOCAL MODES OF THE RANDOM ACCESSIBLE MEMORY

According to the preferred enbodiment of this invention, there are two, global and local, modes for the RAM of a pack. When a local mode is chosen, the content of the RAM is restricted to the (digital) data which is related to that particular pack. Before the pack is mounted to the apparatus, the mode must be local. After the pack is mounted, the RAM has an option to become global mode. On global mode, the CPU can merge, sort the records in this RAM with the global file(s) which contains records of other pack's RAM. This offers a very efficient way to search a record.